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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/565,190	01/20/2006	Masahiro Nomura	Q92733	9238

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EXAMINER	
CHEN, SIBIN	
ART UNIT	PAPER NUMBER
2816	

NOTIFICATION DATE	DELIVERY MODE
07/01/2011	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

sughrue@sughrue.com
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Office Action Summary	Application No.	Applicant(s)	
	10/565,190	NOMURA, MASAHIRO	
	Examiner	Art Unit	
	SIBIN CHEN	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 June 2011*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,6,7,10,11,14,18-26 and 29-35* is/are pending in the application.

4a) Of the above claim(s) *6,7,10,14,20,21,25,26 and 30-35* is/are withdrawn from consideration.

5)☒ Claim(s) *22* is/are allowed.

6)☒ Claim(s) *1-3,18,19,22-24 and 29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 August 2007* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *2/19/2010*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of Species IV, fig. 16, claims 1-3, 18, 19, 22-24, and 29, subspecies II, fig. 18, and subspecies I, fig. 17 in the reply filed on 6/13/2011 is acknowledged.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-3 and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tomita (US Patent# 6,369,627) in view of Asano et al. (JP360030262A).

Regarding claims 1 and 3, fig. 1 of Tomita teaches a multiple-supply-voltage semiconductor device comprising: a clock distribution circuit comprising: at least one first block [8], said at least one first block receiving a clock signal [ICLK]; at least one second block [9]; and at least one variable delay circuit [2] which generates a delayed clock signal [ICLK2] by providing a delay in the clock signal received by the at least one first block; wherein the clock signal [ICLK] received by the at least one first block is different from the delayed clock signal [ICLK2] received by the at least one second block. Tomita does not teach where the first and second blocks receive a variable supply voltage. However, Asano et al. teaches where a frequency divider (the first and

second blocks) is controlled with variable power. In view of such teaching, it would have been obvious to the ordinary artisan at the time the invention was made to modify the invention of Tomita by incorporating the variable power as taught in Asano et al. for the purpose of improving the adjustment of the frequency division ratio. After the incorporation of the aforementioned circuit of Asano et al. into Tomita, the resulting combination teaches a voltage level detector circuit (circuit element in first block receiving the variable power) which detects a voltage level of the variable supply voltage and where said delay changes in accordance with a change in the supply voltage provided to the at least one first block (since the first block controls the delay through control circuits 12-15).

Regarding claim 2, the combination as indicated above teaches wherein said at least one variable delay circuit includes circuitry to increase the delay l as the variable supply voltage decreases.

Regarding claim 29, the combination as indicated above teaches wherein the voltage level detector circuit outputs the detected voltage level as a voltage level detect signal.

4. Claims 18 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tomita in view of Asano et al. in view of Hsu et al. (US Patent# 6,762,957).

Regarding claims 18 and 19, Tomita in view of Asano et al. teaches the device of claim 1 as indicated above. Tomita in view of Asano et al. does not teach where the at least one variable delay circuit comprises a multistage inverter comprising multiple

stacked inverters in series. However, fig. 2 of Hsu et al. shows such a delay with series stacked inverters. In view of such teaching, it would have been obvious to the ordinary artisan at the time the invention was made to modify the invention of Tomita in view of Asano et al. by incorporating the delay design as taught in Hsu et al. for the purpose of implementing the delay circuit with an efficient design.

5. Claims 23 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tomita in view of Asano et al. in view of Welker et al. (US Patent# 7,181,638).

Regarding claim 23, the combination of Tomita in view of Asano et al. as described above in claim 3 teaches the limitations referring to the at least one block, a voltage level detector circuit, and at least one variable delay circuit. Tomita in view of Asano et al. does not teach the details of the delay. However, Welker et al. teaches wherein said at least one variable delay circuit comprises a selector [80] and a delay gate [70A], wherein the delay gate delays the clock signal and the selector outputs to the at least one block either the clock signal or the delayed clock signal generated by the delay gate. In view of such teaching, it would have been obvious to the ordinary artisan at the time the invention was made to modify the invention of Tomita in view of Asano et al. by incorporating the delay design as taught in Welker et al. for the purpose of enabling variable delay amounts for improved control of the circuit.

Regarding claim 24, the combination as indicated above teaches wherein said delay gate comprises at least one inverter (col. 4, lines 50-61).

Allowable Subject Matter

6. Claim 22 is allowed.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to SIBIN CHEN whose telephone number is (571)270-5768. The examiner can normally be reached on Monday to Friday 10:00 to 5:00 eastern.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lincoln Donovan can be reached on (571)272-1988. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

SC
/Lincoln Donovan/
Supervisory Patent Examiner, Art Unit 2816